CLAIMS:

1. Apparatus for controlling direct access to memory circuitry by a device, comprising:

a streaming interface configured to transmit and receive a communication sequence to and from said device;

control logic configured to implement a plurality of direct memory access (DMA) engines configured to read and write data to and from said memory circuitry; and

a set of registers configured to store control data for said plurality of DMA engines.

2. The apparatus of claim 1, wherein said communication sequence comprises a header, a data section, and a footer.

3. The apparatus of claim 2, wherein at least one of said header and said footer includes at least a portion of said control data.

4. The apparatus of claim 1, wherein each of said plurality of DMA engines is configured to read and write said data by processing at least one chain of descriptors, each said at least one chain having at least one descriptor.

5. The apparatus of claim 4, wherein said set of registers comprises, for each of said plurality of DMA engines:

a current descriptor register configured to store a pointer to a descriptor currently processed;

a next descriptor register configured to store a pointer to a descriptor subsequently processed;

a current address register configured to store an address in said memory circuitry associated with a read or write transaction; and

a current length register configured to store a length of data to be read from or written to said memory circuitry.

6. The apparatus of claim 5, wherein each of said plurality of DMA engines is configured to read or write data in response to said current descriptor register receiving a value.

7. The apparatus of claim 4, wherein said set of registers comprises, for each of said plurality of DMA engines:

a status register for storing one or more status flags.

8. The apparatus of claim 4, wherein said set of registers includes an interrupt register, and wherein said control logic is configured to generate an interrupt signal in response to information stored in said interrupt register.

9. The apparatus of claim 1, wherein said memory circuitry comprises double data-rate (DDR) memory circuitry.

10. The apparatus of claim 9, wherein said memory circuitry comprises DDR synchronous dynamic random access memory (SDRAM).

11. A method of controlling direct access to memory circuitry by a device, comprising:

storing control data for direct memory access (DMA) engines;

reading data from said memory circuitry using at least one DMA engine of said DMA engines in response to said control data; and

transmitting a communication sequence to said device over a streaming interface, said communication sequence including said data.

12. The method of claim 11, wherein said communication sequence comprises a header, a data section, and a footer.

13. The method of claim 12, wherein at least one of said header and said footer includes at least a portion of said control data.

14. The method of claim 11, further comprising:

forming, for each said at least one DMA engine, a chain of descriptors having at least one descriptor.

15. The method of claim 14, wherein said control data comprises, for each said at least one DMA engine, a pointer to a first descriptor in said chain of descriptors, a next descriptor in said chain of descriptors, an address in said memory circuitry associated with a read transaction, and a length of data to be read from said memory circuitry.

16. The method of claim 15, wherein said step of reading from said memory is performed in response to said pointer to said first descriptor for each said at least one DMA engine.

17. The method of claim 15, wherein said control data further comprises, for each said at least one DMA engine, status data having one or more status flags.

18. The method of claim 15, wherein said control data further comprises interrupt data.

19. The method of claim 18, further comprising:

interrupting a processor in response to said interrupt data.

20. A method of controlling direct access to memory circuitry by a device, comprising:

receiving a communication sequence from said device over a streaming interface, said communication sequence including

data to be written to said memory circuitry;

storing control data for direct memory access (DMA) engines; and

writing said data to said memory circuitry using at least one DMA engine of said DMA engines in response to said control data.

21. The method of claim 20, wherein said communication sequence comprises a header, a data section, and a footer.

22. The method of claim 21, wherein at least one of said header and said footer includes at least a portion of said control data.

23. The method of claim 21, further comprising:

forming, for each said at least one DMA engine, a chain of descriptors having at least one descriptor.

24. The method of claim 23, wherein said control data comprises, for each said at least one DMA engine, a pointer to a first descriptor in said chain of descriptors, a next descriptor in said chain of descriptors, an address in said memory circuitry associated with a write transaction, and a length of data to be written to said memory circuitry.

25. The method of claim 24, wherein said step of writing to said memory is performed in response to said pointer to said first descriptor for each said at least one DMA engine.

26. The method of claim 24, wherein said control data further comprises, for each said at least one DMA engine, status data having one or more status flags.

27. The method of claim 24, wherein said control data further comprises interrupt data.

28. The method of claim 27, further comprising:

interrupting a processor in response to said interrupt data.

29. A data processing system, comprising:

a processor;

memory circuitry;

a peripheral device; and

a direct memory access (DMA) controller, comprising:

a streaming interface configured to transmit and receive a communication sequence to and from said peripheral device;

control logic configured to implement a plurality of direct memory access (DMA) engines configured to read and write data to and from said memory circuitry; and

a set of registers configured to store control data for said plurality of DMA engines.

30. The system of claim 29, wherein said communication sequence comprises a header, a data section, and a footer.

31. The system of claim 30, wherein at least one of said header and said footer includes at least a portion of said control data.

32. The system of claim 29, wherein said processor is configured to store at least one chain of descriptors in said memory circuitry, each said at least one chain having at least one descriptor, and wherein each of said plurality of DMA engines is configured to read and write said data by processing said at least one chain of descriptors.

33. The system of claim 29, wherein said memory circuitry comprises double data-rate (DDR) memory circuitry.

34. The system of claim 33, wherein said memory circuitry comprises DDR synchronous dynamic random access memory (SDRAM).

35. The system of claim 29, wherein said DMA controller is disposed within an integrated circuit.

36. The system of claim 35, wherein said integrated circuit comprises a programmable logic device, and wherein said DMA controller is implemented using programmable logic of said programmable logic device.